A Novel Silicon High Voltage Vertical MOSFET Technology for a 100W L-Band Radar Application

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Abstract — **The silicon vertical MOSFET RF power amplifier described in this paper is the industry's first to utilize high voltage vertical technology. Operating under pulse conditions of 200µsec pulse width and 10% duty cycle it delivers more than 100W of peak power. Operating in Class AB with only 50mA of bias current the device achieves more than 20dB of gain and 47% power added efficiency at P1dB compression across 200MHz of bandwidth at L-Band from 1.2GHz to 1.4GHz. The DC characteristics include a BVdss of 115 volts enabling high voltage operation with a 48V power supply.**

I. INTRODUCTION

The HVVFET™ (High Voltage Vertical Field Effect Transistor) is an advanced vertical MOSFET structure that expands the operating frequencies of vertical silicon RF power MOSFETs well into the microwave spectrum. The device architecture also yields an extremely rugged device by suppressing the activation of the parasitic device that destroys other pulsed transistors. The HVVFET is rated at 20:1 VSWR with an operating voltage of 48V. Other device attributes such as gain and efficiency are described in this paper. One example of an application that is addressed by the new transistor is in L-Band pulsed radar systems.

Two common methods of achieving high output power are increasing gate periphery and increasing operating supply voltage. Increasing the gate periphery for higher output power reaches a point of diminishing return because of the reduction in output impedance. High voltage operation has several benefits:

1) transistors operating at higher voltages dissipate less heat due to lower current consumption at a given power level;
2) transistor impedances increase with higher voltage operation, making it easier to design an effective impedance matching network; and
3) higher output impedances aid wider bandwidth designs.

One key aspect of a vertical MOSFET is that the current flows vertically in the drain region while, conversely, in a LDMOS structure the current flow is lateral. The vertical current flow allows the transistor cells of the device to be tightly spaced. The architecture of the HVVFET is optimized for this attribute yielding a power density approximately 3 times that of an equivalent lateral transistor device (e.g. LDMOS). The increased power density allows high power components to be fitted into the smallest package footprint.

Avionics and military pulsed applications have traditionally used bipolar transistors as the primary device technology because of their high power capability. Modern system requirements are demanding additional transistor performance. Electrical performance improvements in the HVVFET technology such as higher power density, increased gain and better gain flatness offer significant benefits to power amplifier designers, and will produce higher performance amplifiers having reduced size and weight.

This technology offers many system level advantages. The gain of the device is at least 3dB greater than competitor devices which reduces the driver output power requirement by 50%. The combination of high power packing density and smaller driver output power reduces both the size of the PCB and the heatsink and cooling requirements. The extreme ruggedness of the transistor and the inherent reliability of a silicon based technology leads to lower field failure rates and a reduction in maintenance cost. All of the above factors improve system performance and lower total system cost.

II. VERTICAL MOSFET TECHNOLOGY

The HVVFET device is fabricated using standard silicon wafer process technologies. The performance of the device is enhanced by using a number of innovative features which are briefly described. The high operation voltage of the device is enabled by using a vertical configuration that uses the epi thickness to determine the breakdown voltage while maintaining small cell pitch on the top device structure, thereby achieving high power density without sacrificing performance. By utilizing an innovative termination scheme, near ideal planar breakdown voltages are achieved while using the optimal epi doping and thickness to reduce $R_{DS(on)}$. The feedback capacitance of the device is reduced significantly by using an integrated device shield to minimize the coupling of the gate to the drain. In addition, by utilizing the same shield structure, the intrinsic and extrinsic feedback capacitance is reduced by a factor of 20 compared to similar vertical devices.

III. DEVICE CONFIGURATION

This single-ended high power transistor is a first-generation HVVFET device. The discrete silicon N-Channel enhancement mode transistor is implemented in common source configuration for high power operation.

The single die is attached directly to the flange material allowing the generated heat to be quickly extracted to the heatsink for maximum thermal performance. An optimized die attach process is achieved without solder preforms. Based upon simulations and measured results the thermal resistance of the package part is 0.85°C/W.

The device is housed in a RF high power bolt-down package with an industry standard HV400 footprint as shown in Figure 1. The package can be mounted with screws or soldered to the heatsink for optimum attach to the thermal interface.

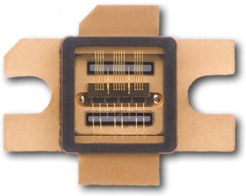

Fig. 1 HV400 Power Package

IV. MATCHING NETWORKS

The internal matching networks within the device package transform the low impedance of the die to higher impedance at the terminal leads of the package. The matching networks are designed to achieve a minimum 15% fractional bandwidth performance at 1300MHz. At any given power level the high drain voltage bias scheme creates higher devices impedances than similarly power rated devices. The nature of the vertical device structure produces low intrinsic capacitances. The inherently low input and output die capacitance makes the device easy to match. In fact, only a single stage of input and output matching is required internal to the package as seen in Figure 2. All matching is done using reliable gold wires. A single matching section of a low pass network is formed at the input with wire LG1 shunted to ground through MOS capacitor C1. The series wires LG2 connect the low pass filter to the gate terminal of the die. The output impedance match is realized by bonding wires from the drain of the transistor to a large MOS capacitor which acts as a DC block. Intrinsic die output capacitance is resonated with inductance LD2 which are shunted to ground. The MOS capacitor C2 in series with the shunt LD2 wires allows only RF current to flow to ground effectively presenting high impedance to low frequency and DC components of the current. The simple, single-plate MOS capacitors are easy to manufacture, low cost and are the only additional elements internal to the package. The internal matching effectively allows the device to achieve flat gain and efficiency and the IRL response across the 200MHz bandwidth at the high end of the L-Band.

The wirebond profiles are not complicated, allowing the devices to be manufactured accurately and repeatably, using automatic wirebonders. The wires are evenly spaced for uniform current distribution preventing thermal issues such as hotspots on the die resulting from phase mismatching.

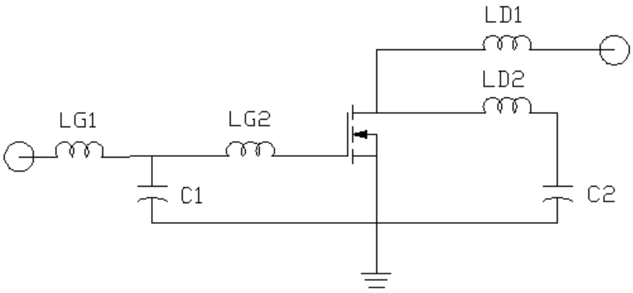

Fig. 2 Schematic Diagram of the Input and Output Matching Networks

The single-ended input and output impedances achieved with the low-loss internal matching elements are listed in Table 1. External matching was accomplished through lumped elements on a PCB raising the impedance to 50 ohms.

TABLE I
SUMMARY OF PACKAGED DIE IMPEDANCES

Frequency	Zin	Zout
1200 MHz	2.9-j4.1	6.3-j4.2
1300 MHz	2.5-j2.8	5.8-j2.5
1400 MHz	2.2-j0.8	5.6-j0.9

V. RF PERFORMANCE CHARACTERISTICS

The test fixture was optimized for pulsed power performance from 1200MHz to 1400MHz. At least 15% of fractional bandwidth was attained, centered at 1300MHz. the transistor was matched not only for high power performance metrics but also for frequency response. The test circuit was tuned with microstrip lines and surface mount chip components for flat gain and efficiency across the frequency band of operation. Figures 3 and 4 show the flat response of the device over frequency.

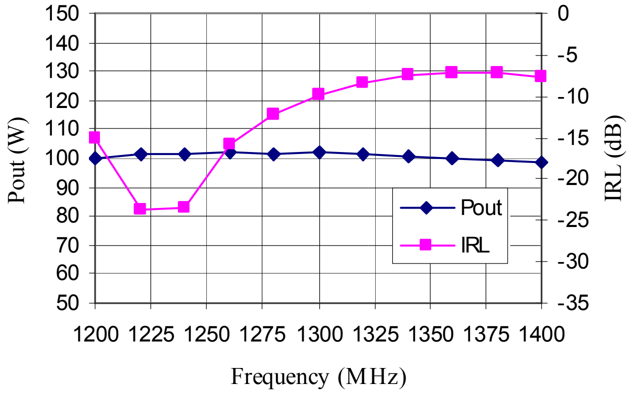

Fig. 3 Measured RF performance of peak output power and input return loss over frequency taken with pulsed signal conditions of 200µsec pulse width, 10% duty cycle, VDD = 48V, Class AB bias circuit. Peak output power exceeds 100W across the band with minimum 47% power added efficiency.

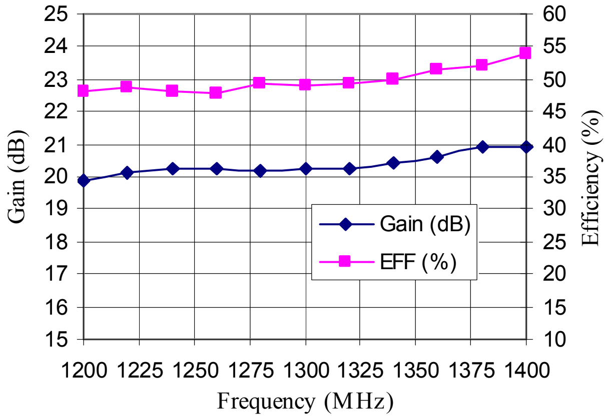

Fig. 4 Measured RF performance of gain and efficiency versus frequency taken with pulsed signal conditions of 200μsec pulse width, 10% duty cycle, VDD = 48V, Class AB bias circuit. Gain exceeds 20dB and is less than 1dB flat across 200MHz of bandwidth.

The device achieves greater than 20dB of gain at the P1dB compression point. At this power level the power transistor delivers greater than 50% drain efficiency. With gain as high as 20dB the power added efficiency is essentially the same as the drain efficiency since the required input power level is so small compared to the output power. [1]

High power design is rigorous since not only are high power performance metrics such as peak power, gain and efficiency important but this performance must be achieved over an entire frequency band of operation. The gain flatness is less than 1dB and will meet the minimum system specification without having additional circuitry like AGC (automatic gain control) modules to compensate the system gain. The flat efficiency response results in constant power supply consumption. The balanced power consumption prevents any fluctuations in the power supply lines, resulting in stable performance.

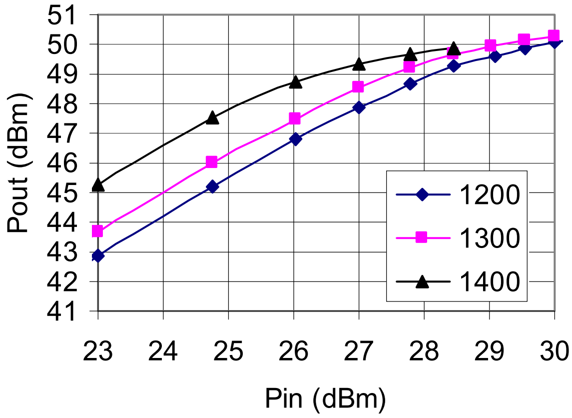

Fig. 5 Output power versus input power at VDD = 48V under pulsed conditions: 200μsec pulse width, 10% duty cycle.

The device achieves over 100W of peak power at 200μsec pulse width and 10% duty cycle. Figure 5 shows the performance over power drive displaying the linear range of operation and driving into the saturation region.

One of the most challenging test conditions for any RF transistor is being able to handle load mismatches at all phases as in [2]. Under nominal operating voltage of 48V at rated power, the device is able to withstand a 20:1 VSWR without exhibiting any lasting performance degradation.

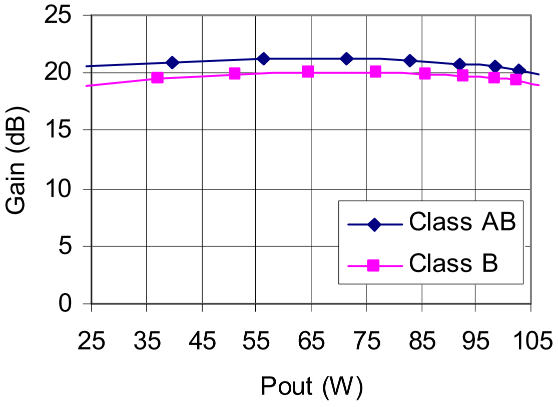

Fig. 6 Measured gain flatness across output power at 1300MHz with VDD = 48V and pulse signal conditions of 200μsec pulse width, 10% duty cycle, showing Class B versus Class AB bias levels.

Figure 6 displays the gain which is greater than 20dB with Class AB current bias. When biased in class B mode for high efficiency applications the device maintains the high gain characteristic of the classical Class AB mode of operation. The advantage of the Class B design is that the high efficiency approach draws zero current and consumes zero power when the transmitter is off. The Class AB bias scheme has higher gain but consumes DC power throughout the pulse cycle without regard to whether the RF signal is applied or not. [3] The HVVFET technology maintains gain above 20dB across the band at Class B which maximizes efficiency.

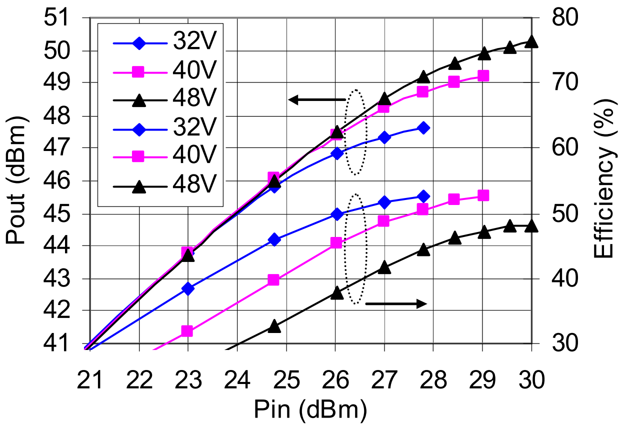

Fig. 7 Measured output power at 1300MHz, VDD = 48V with pulse signal 200μsec pulse width and 10% duty cycle displaying performance across varying voltage supply bias.

Figure 7 shows the tradeoffs of voltage bias supply and RF performance. It is clear that a lower operating voltage achieves greater efficiency at the cost of maximum output power. Some applications may require higher efficiency and are willing to sacrifice some power in order to attain the proper system specification. The device gain is not affected by variations in the drain power supply.

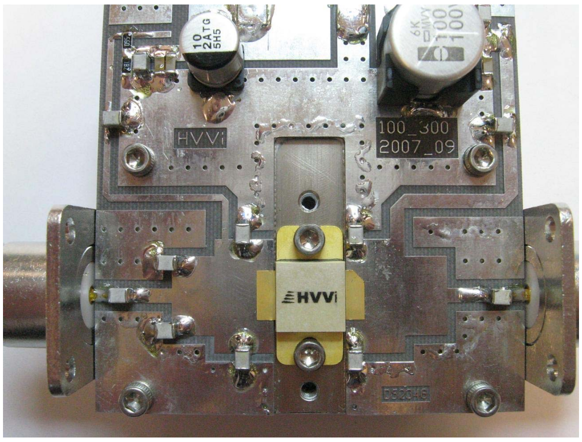

Fig. 8 Picture of the test fixture matching at L-Bamd

The external matching circuitry covers over 200MHz of bandwidth in a single printed circuit board. Figure 8 shows the external input and output matching networks which are comprised of a combination of both microstrip transmission lines and lumped elements. The power gain flatness is less than 1.0dB across the frequency band. On the DC bias lines of both the gate and drain are large capacitors in the μF range that suppress the low frequency components on the DC supply lines preventing stability issues. RF shunt capacitors are placed at one quarter of a wavelength of the fundamental frequency away from the leads of the device to isolate the DC bias feed line from the RF impedance matching network. These capacitors presents a null or low impedance at the fundamental frequency shunting the residual RF signal to ground with the capacitor effectively isolating the DC current. DC blocking capacitors on the RF lines isolate the bias supply from the connectors.

The high impedance at the package leads, because of the internal matching, makes the test fixture circuit easy to match to 50 ohms. The match does not require expensive high dielectric material but uses low cost standard dielectric material from Rogers Corporation, resulting in a significant cost savings. The use of only standard values of capacitance for the piece parts (chip capacitors) for both RF match and DC bias networks results in a cost effective solution.

VI. FUTURE ROADMAP

Simulations indicate that higher performance at frequencies as high as 10GHz and breakdown voltages exceeding 200V are feasible with the HVVFET structure once optimized layout for CW and linear applications is pursued. The performance advantages achievable with future generations of HVVFETs make it a likely candidate for many high power RF and microwave applications.

VII. CONCLUSIONS

The HVVFET is the first new silicon high frequency RF power transistor introduced in more than a decade. This paper described a unique approach to high power amplifier design utilizing technological breakthroughs that result in increased RF performance and many system benefits. The first generation of this technology demonstrates state-of-the-art performance with a clear path to higher breakdown voltages to enhance performance advantages in future generations.

ACKNOWLEDGMENT

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