

High Performance Vertical MOSFET Technology Enables Phased Array Radar Applications

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Abstract— The silicon vertical MOSFET RF power amplifier described in this document is one of the industry’s first to utilize high voltage vertical technology. The power amplifier produces more than 25W of peak pulsed power in the L-Band from 1200MHz to 1400MHz for ground based radar applications. Exhibiting nearly 20dB of gain, 50% efficiency at 48 volt operation with a 200µsec pulse width and 10% duty cycle conditions produces high performance in a surface mount package that is less than 200 mils square. Cross sections of the device architecture as well as the high device impedances achieved are shown. The effects of varying the drain voltage and current are also explored.

I. INTRODUCTION

A new series of high voltage RF Power MOSFETs targeting L-Band pulsed applications has been introduced. The HVVFET™ (High Voltage Vertical Field Effect Transistor) is an advanced vertical MOSFET structure. The HVVFET structure discussed in this paper stands off a minimum breakdown voltage of 115 volts which allows operating voltages as high as 48 volts. The device exhibits high breakdown voltage that withstands the high voltage swings present during many pulsed applications. The vertical architecture yields an extremely rugged device and is rated at a 20:1 VSWR even with an operating voltage of 48 volts. [1] The high operating voltage also allows a driver stage of up to 25W to be used in a line-up utilizing higher power devices with both parts sharing the same power supply.

The unique transistor architecture exhibits a high device power packing density which allows the devices to be placed in a smaller package dimension than other available product offerings. One example of an application where the increased packing density and high operating voltage offers system level advantages is in phased array radar. The physically small size of this package and the pick and place assembly capability enable this device to drive phased array radar applications which use many devices in parallel to produce very high output power levels. Phased array radar systems sometimes use more than a thousand transistors in parallel to achieve the 10’s of kilowatts of output power necessary in the radar application. The physical size of the device when using so many in parallel is a critical factor in determining whether the high power levels can be achieved in a physically realizable space.

II. VERTICAL MOSFET TECHNOLOGY

The HVVFET device is fabricated using industry standard wafer processing techniques. The performance of the device is enhanced by using a number of innovative features which are briefly described. The device is formed on a layer of epitaxial silicon grown on top of a heavily doped substrate. The high operating voltage of the device is enabled by using a vertical configuration that uses the epi thickness to determine the breakdown voltage while maintaining small cell pitch on the top device structure, thereby achieving high power density without sacrificing performance. The gate length is defined using spacer technology that enables a short gate length device with linear I-V characteristics. The thickness and the doping level of the epi layer is optimized to reduce $R_{DS(on)}$ while near ideal planar breakdown is achieved through a novel termination scheme. Figure 1 shows a cross-sectional SEM of the device after the sidewall gate has been formed.

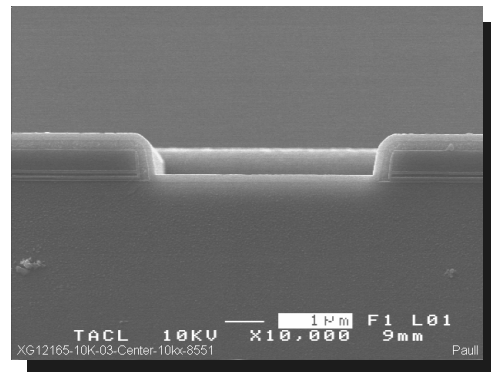


Fig. 1 Cross-sectional SEM of HVVFET Vertical Device Structure

Figure 2 shows a top view of the array of micro-cells forming a distributed transistor structure. The annular source opening enables the increase of the device perimeter in a compact manner thereby allowing significant packing density. The feedback capacitance of the device is reduced significantly by using an integrated device shield to minimize the coupling of the gate to the drain device terminals. In addition, by utilizing the same shield structure, the intrinsic

and extrinsic feedback capacitance is reduced by a factor of 20 compared to similar vertical devices allowing operating frequencies beyond the L-Band.

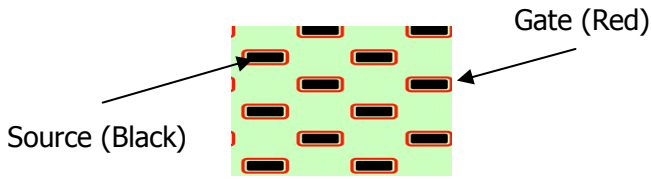


Fig. 2 Mesh Device Structure viewed from the Source-Gate surface

III. DEVICE PACKAGE

This single-ended high power transistor is a first generation HVVFET device. The discrete silicon N-Channel enhancement mode transistor is implemented in common source configuration for high power operation.

The single discrete die pictured in Figure 2 is flip-chip mounted to a dielectric package board with appropriate contact to the Source and Gate mesh. The Drain (on the backside of the chip) is wire bonded to the package board. Vias in the package board shunt the heat generated during the operation of the part to the bottom of the package, which is then soldered directly to the circuit board for the application. The device can be handled during assembly with a high volume pick and place automated assembly line which saves assembly and back end manufacturing costs significantly. The 20 mil thick aluminium nitride material closely matches the thermal expansion properties of the silicon die. Unlike bipolar technology which commonly uses a BeO dielectric carrier and is harmful to the environment, the AlN material passes the rigorous ROHS standard.

Although this silicon active device is rated at a maximum operated junction temperature of 200°C many customers derate that value to 150°C for long-term reliability concerns. The thermal resistance is measured to be 2.5°C/W under pulse conditions of a 200 μsec pulse width and 2 msec pulse period. At 48V operating supply the device produces 25W of output power and is 50% efficient therefore producing 25W of energy that must be dissipated within the device. From this data, the temperature rise of the device under test is calculated to be 62.5°C. Starting with a maximum case temperature of 85°C these characteristics create a maximum junction temperature of 147.5°C well below even the de-rated maximum temperature specification.

The device is housed in a RF high power surface mount package with a footprint that is less than 200 mils square. The device when mounted is soldered to the heatsink for optimum attach to the thermal interface. The physical dimensions of the device package are shown in Fig. 3.

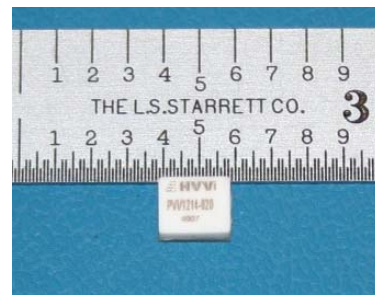


Fig. 3 Surface Mount Power Package

IV. IMPEDANCE VALUES

Another benefit of the high operating voltage is the higher load impedance that is required to achieve optimum match to the device. The intrinsic input and output capacitances of the 25W HVVFET are low enough that no additional internal matching is required within the device package. The unmatched device has high enough impedances to match the leads of the device to 50 ohms on a printed circuit board that is 6.4 cm (=2.5") square using a Teflon dielectric material with a low dielectric constant. A smaller matching circuit can be obtained using a material with a higher dielectric constant although the material is more expensive. [2] The single-ended unmatched input and output impedances achieved by the package part are listed in Table 1.

TABLE I
SUMMARY OF PACKAGED DIE IMPEDANCES

Frequency	Zinput	Zoutput
1200 MHz	1.4-j2.6	6.6-j3.9
1300 MHz	1.3-j2.7	7.2-j4.3
1400 MHz	0.9-j2.6	6.8-j3.8

V. RF PERFORMANCE CHARACTERISTICS

The RF performance of the device was measured in a test fixture matched to 50 ohms on a 6.4cm by 6.4cm Arlon Teflon printed circuit board.

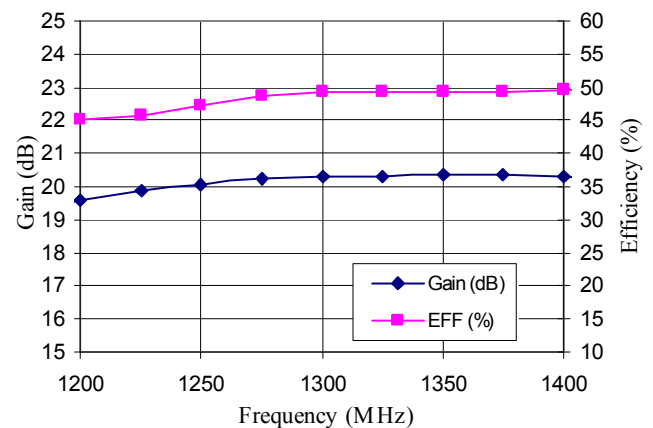


Fig. 4 Narrowband RF gain and efficiency versus frequency. Performance measured with pulsed signal conditions of 200μsec pulse width, 2msec pulse period and VDD = 48V. Gain exceeds 19dB with less than 1.5dB flatness across the band.

The device achieves a minimum of 45% of drain efficiency across the frequency band of interest. The device produces 25W of output power with gain ranging from 19.6dB to 20.3dB at the P1dB compression point. Ground based radar applications in the L-Band require frequency response from 1200MHz to 1400MHz. Variability in wafer processing and the assembly process during manufacturing make meeting today's power amplifier design stringent specifications difficult. Therefore it is necessary to design products that perform well outside of the application specified band of operation.

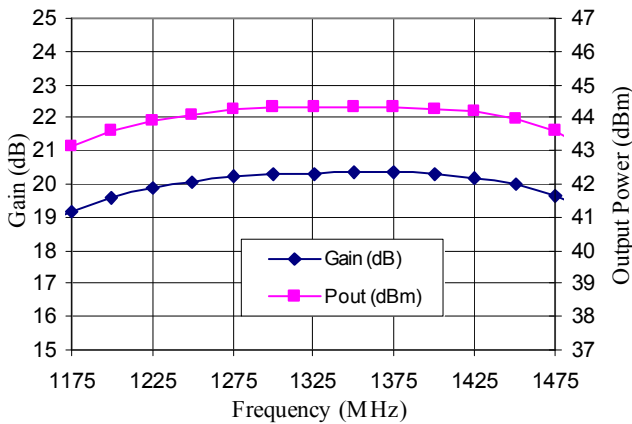


Fig. 5 Wideband RF Performance of gain and efficiency versus frequency. Performance measured with pulsed signal conditions of 200µsec pulse width and 2msec pulse period and VDD = 48V. Gain exceeds 19dB with less than 1.5dB flatness across the band.

Figure 5 shows the wideband performance of the device. The device is able to deliver more than 20W of P1dB output power across more than 300MHz. The gain flatness is still maintained at less than 1.5dB across this frequency band of operation. The fractional bandwidth now exceeds 20% while still delivering more than 19dB of gain and efficiencies greater than 40%.

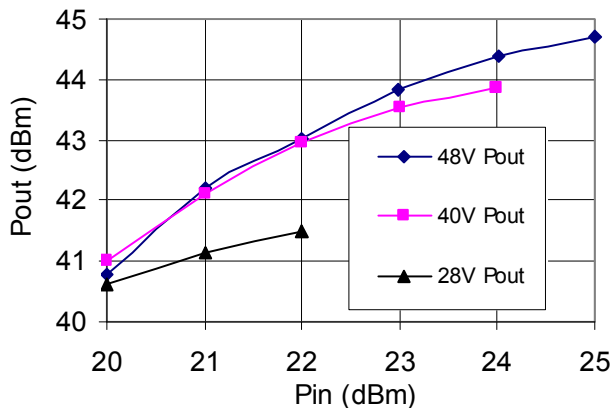


Fig. 6 Output power versus input power with varying drain supply voltage. Performance measured with pulsed signal conditions of 200µsec pulse width, 2msec pulse period and VDD = 48V.

The effect of varying the drain supply voltage bias is shown in Figure 6. The device was optimized for high power operation with a 48 volt power supply connected to the drain bias. At the 48 volt level the device is capable of 30W output power at P1dB compression. The device produces more than 25W of power with the voltage bias reduced to 40 volts. The device still is capable of delivering half of the output power at the 28 volt bias level. The P_{OUT} vs P_{IN} performance results reported in Figure 6 correspond to a load line that is optimized for maximum power and efficiency at 48 volt operation. Approximately 3dB of power is lost when reducing the drain voltage by nearly a factor of 2. Figure 7 shows an example of the trade-offs in performance of gain, power and efficiency.

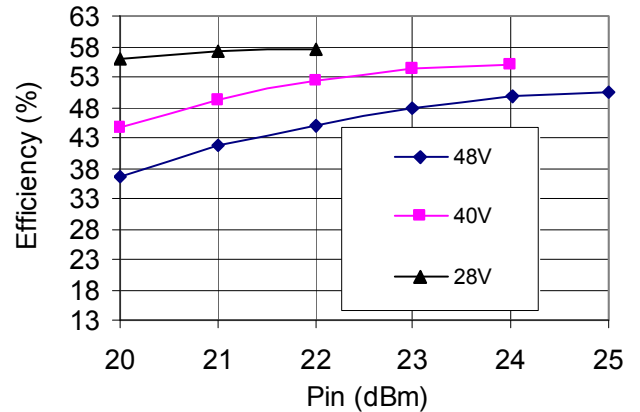


Fig. 7 Efficiency versus input power with varying drain supply voltage. Performance measured with pulsed signal conditions of 200µsec pulse width and 2msec pulse period and VDD = 48V.

At the P1dB compression point the device, operating under 48 volt operation, has 50% efficiency. Many applications require highly efficient operation. Figure 7 shows the benefits of reducing the output power to gain fairly significant levels of efficiency. Operating at 40 volt drain bias the device will exceed 54% efficiency and at 28 volt drain bias the device is better than 57% efficient.

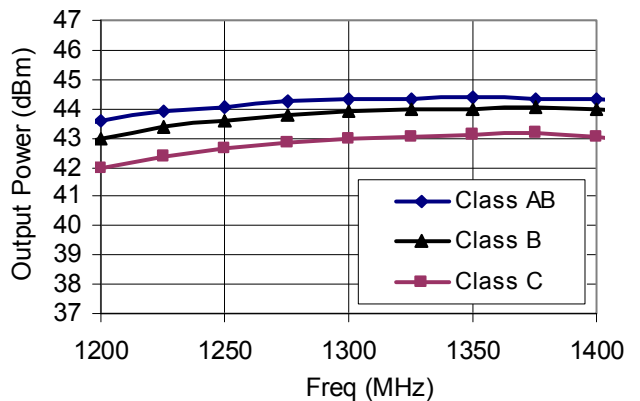


Fig. 8 Output power versus frequency with varying quiescent current bias levels. Performance measured with pulsed signal conditions of 200µsec pulse width and 2msec pulse period and VDD = 48V.

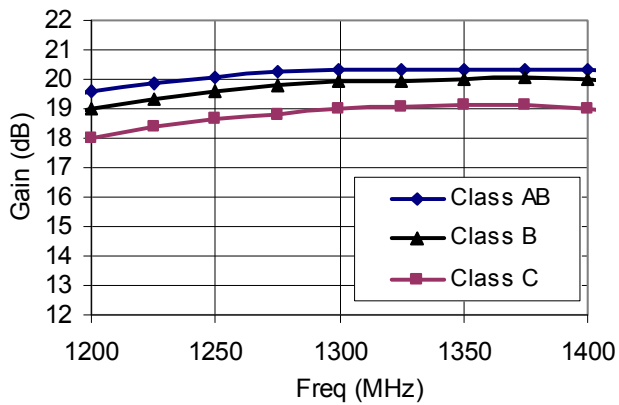


Fig. 9 Gain versus frequency with varying quiescent current bias levels. Performance measured with pulsed signal conditions of 200 μ sec pulse width and 2msec pulse period and VDD = 48V.

Figures 8 and 9 shows the effect of operating the device under varying classes of operation. [3] The DC bias voltage on the gate terminal is set to exactly match the threshold voltage of the active device in Class B operation. The RF signal will activate the device for half of the period of the ac signal in this mode of operation. In Class AB the device is active for more than half of the period of the applied RF signal and exhibits more gain and output power than the other bias levels shown in this example. The HVVFET has been characterized in Class AB mode of operation. In Class C the bias voltage level is reduced which will cause the device to be active for less than half of the period of the applied RF signal. Although Class C operation has approximately 1.5dB less gain and output compared to Class AB in this example, it also is the most efficient mode of operation drawing no current when the RF signal pulse is not being applied to the input of the device. The performance trade-offs between the RF parameters of gain, output power and efficiency are similar to the effect of varying the voltage bias on the drain terminal.

VI. CONCLUSIONS

The first generation of this device and packaging technology demonstrates state-of-the-art performance for power levels up to 25W in the L-Band. The HVVFET has already been demonstrated to be attractive for applications at power levels as high as 100W, but such performance requires alternate packaging approaches to that discussed in this paper. [4] High gain and efficiency were described across a fractional bandwidth greater than 20%. The high power packing density was demonstrated as the device resides in the industry's smallest package for this output power level. The unique package can enable phased array radar applications both with its small physical size and its ability for high volume manufacturability. The high voltage capability of the device enables the power supply to remain at a single level across each stage of a power device line-up. The high voltage also creates high impedance for the device which is unmatched internally saving additional cost.

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